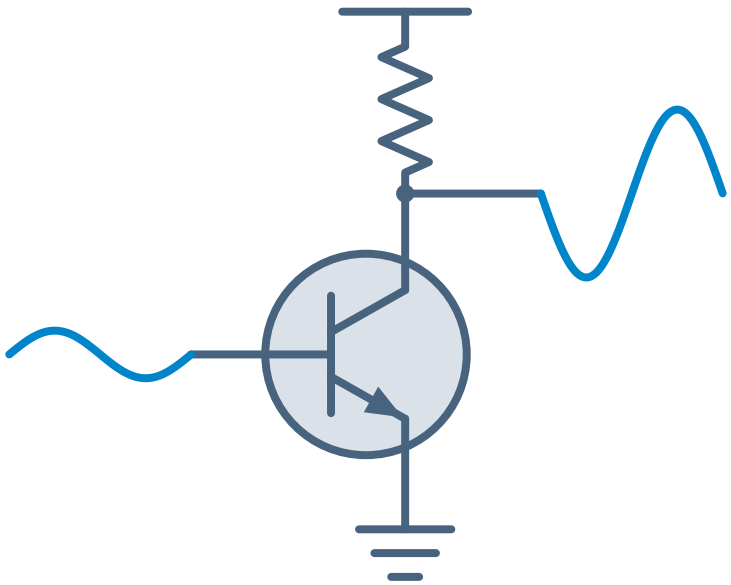
ELECTRONICS 1

PROBLEM BOOK

SAMPLE PAGES

11 chapters · 150 problems · step-by-step solutions



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How to use this book

- Each chapter opens with a reminder box summarizing the definitions and formulas the problems rely on.
- Difficulty: ★☆☆ basic ★★☆ intermediate ★★★ advanced. Each chapter has a few multiple-choice concept questions; its last problem is an exam-style mixed problem combining several topics.
- The dotted area below each problem is for your own work. Solve first; if stuck, go back to the reminder box and the lecture notes, and look at the solution last.
- All solutions are at the end of the book. The Solution → link next to a problem takes you to its solution, and ← Problem takes you back. Short answers are in the **ANSWER** box. Where needed, a solution begins with its assumptions and names the appendix tables it uses; amplifier solutions include a figure of the small-signal equivalent circuit.
- **Appendix tables:** Semiconductor constants, diode, BJT and MOSFET parameters, a small-signal summary, standard resistor and capacitor values (E12, E24), and decibel and Bode rules are in the appendix at the end of the book. Problems are solved with this appendix and the problem data only; a parameter not given takes its default value from the appendix.
- **Notation and defaults:** The total instantaneous value is written i_C, the dc value I_C, the small-signal value i_c and its amplitude I_c. Unless stated otherwise, $V_T = 25$ mV, $V_{BE(\text{on})} = V_{D(\text{on})} = 0.7$ V, $V_{CE(\text{sat})} = 0.2$ V, $V_A = \infty$ and $\lambda = 0$. Each dc solution starts from an assumed operating region and checks that assumption at the end.
- **Shared chapter:** Chapter 11 (frequency response) also appears in *Electronics 2*, for schools whose second course begins with this topic.
- **Reading order:** The book starts with the BJT (Chapters 5–7) and moves on to the MOSFET (Chapters 8–9). If your course starts with the MOSFET, study Chapters 1–4, 8–9, 5–7 and 10–11 in this order: the problems in Chapters 8–9 do not require BJT material, and the problems that compare the two transistors are only in the *Mixed problems* sections of these chapters. Semiconductor physics (Chapter 2) is kept short.
- **Midterm and final:** The midterm usually covers diodes and the dc analysis of the BJT (Chapters 1–6); the final covers the whole book. The order and scope of topics vary from school to school; choose the chapters to study according to your own course syllabus. You can also verify the results with a circuit simulation program.

Contents

Page numbers refer to the full book. Chapters in color are in this sample; click to go there.

1 Amplifier Fundamentals and the Ideal Op Amp ..... 10 problems 4
2 Semiconductors and the pn Junction ..... 10 problems 11
3 **Diode Models and Diode Circuits** ..... 14 problems 17
4 Diode Applications: Rectifiers, Zener Regulators, Limiters and Clampers ..... 16 problems 25
5 The BJT: Structure, Modes of Operation and DC Analysis ..... 14 problems 34
6 **BJT Biasing and Bias Stability** ..... 12 problems 42
7 Small-Signal BJT Amplifiers ..... 18 problems 50
8 **MOSFETs and JFETs: Structure, Characteristics and DC Analysis** ..... 14 problems 65
9 Small-Signal FET Amplifiers ..... 16 problems 73
10 Introduction to Multistage Amplifiers: Cascade, Darlington, Cascode ..... 10 problems 86
11 Frequency Response of Single-Stage Amplifiers ..... 16 problems 95

Solutions 107

Appendix: Tables 178

CHAPTER 3

DIODE MODELS AND DIODE CIRCUITS

ideal diode on: $v_D = 0,\ i_D > 0$; off: $i_D = 0,\ v_D < 0$

exponential model $i_D = I_S\left(e^{v_D/(nV_T)} - 1\right) \approx I_S\, e^{v_D/(nV_T)}$

voltage difference at two currents $V_2 - V_1 = nV_T \ln \dfrac{I_2}{I_1}$

constant drop, piecewise linear $v_D = V_{D0}$; $v_D = V_{D0} + r_D\, i_D$

small-signal resistance $r_d = \dfrac{nV_T}{I_D}$

small-signal condition $|v_d| \ll nV_T$ $(|v_d| \le 5\text{ mV})$

load line $i_D = \dfrac{V_{DD} - v_D}{R}$

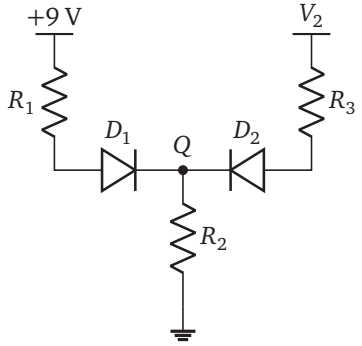
temperature (at constant current) $\dfrac{dV_D}{dT} \approx -2\text{ mV/K}$

A total instantaneous quantity is written with a lowercase symbol and an uppercase subscript (i_D), a dc quantity with an uppercase symbol and an uppercase subscript (I_D), a small signal with a lowercase symbol and a lowercase subscript (i_d), and the peak value of a small signal with an uppercase symbol and a lowercase subscript (I_d). Unless stated otherwise, Si diodes are modeled with the constant-voltage-drop model: when on, $v_D = V_{D0} = 0.7$ V. An "ideal diode" is taken to have $v_D = 0$ when on. In the exponential model $V_T = 25$ mV; I_S and n are in Table E-2 (small-signal Si diode: $I_S = 10^{-15}$ A, $n = 1$). Every solution starts by assuming the states of the diodes (on or off) and checks them at the end: an on diode must have $I_D > 0$, and an off diode $V_D < V_{D0}$ ($V_D < 0$ for an ideal diode). The diode voltage is measured from anode to cathode, and its current from anode to cathode. Resistances are in kilohms, currents in milliamperes and voltages in volts.

Ideal diode and assumed states

3.3 ★★☆ Solution →

In the circuit shown, D_1 and D_2 are ideal diodes; $R_1 = 1.5\text{ k}\Omega$, $R_2 = 2.2\text{ k}\Omega$, $R_3 = 1\text{ k}\Omega$ and $V_2 = 4$ V.



a. Assuming both diodes are on, find V_Q and the diode currents; state whether the assumption holds.

b. Determine the correct states of the diodes and find V_Q and I_{D1}.

c. What value (in volts) must V_2 exceed for D_2 to turn on?

Exponential, constant-drop and piecewise-linear models

3.4 ★☆☆ Solution →

Assume that the small-signal Si diode of Table E-2 ($I_S = 10^{-15}$ A, $n = 1$) operates in the forward direction.

a. Find the diode voltages at $I_D = 0.2$ mA and $I_D = 5$ mA.

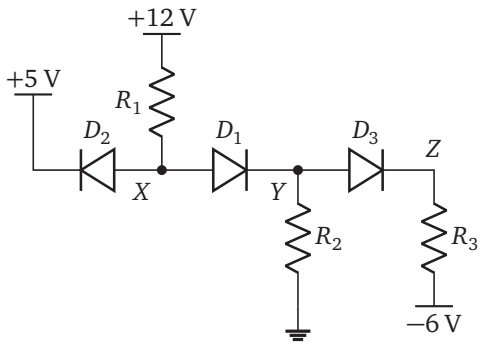
b. By how many mV does the diode voltage increase when the current increases by a factor of 10?

c. If the diode voltage is increased by 30 mV, by what factor does the current increase?

Multi-diode circuits and diode logic gates

3.12 ★★★ Solution →

In the circuit shown, $R_1 = 2.2$ kΩ, $R_2 = 3.3$ kΩ and $R_3 = 4.7$ kΩ; the rails are +12 V, +5 V and −6 V.



a. Assuming all three diodes are on, find the diode currents and show that the assumption does not hold.

b. Determine the correct states and find the voltages V_X, V_Y, V_Z and the currents of the on diodes.

c. Below what voltage must the +5 V rail fall for D_2 to turn on as well?

CHAPTER 6

BJT BIASING AND BIAS STABILITY

single base resistor $I_B = \dfrac{V_{CC} - V_{BE}}{R_B}, \quad I_C = \beta I_B$

collector-to-base feedback $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}$

Thévenin equivalent of the base divider

$V_{\text{Th}} = V_{CC}\dfrac{R_2}{R_1 + R_2}, \quad R_{\text{Th}} = R_1 \parallel R_2$

dual supply (R_B from base to ground)

$I_B = \dfrac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$

divider and R_E $I_B = \dfrac{V_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$

DC load line $V_{CE} = V_{CC} - I_C R_{\text{dc}}, \quad R_{\text{dc}} = R_C + \dfrac{R_E}{\alpha}$

insensitivity to β variation $\dfrac{R_{\text{Th}}}{\beta + 1} \ll R_E$

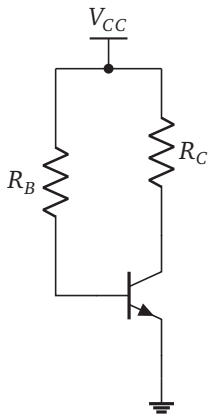
percentage change $\dfrac{\Delta I_C}{I_C} = \dfrac{I_{C2} - I_{C1}}{I_{C1}}$

The dc quantities are written with an uppercase letter and uppercase subscript (I_C, V_{CE}). Unless stated otherwise, $V_{BE(\text{on})} = 0.7\ \text{V}$, $V_{CE(\text{sat})} = 0.2\ \text{V}$ (for the pnp, $V_{EB(\text{on})}$ and $V_{EC(\text{sat})}$ with the same values) and the Early effect is neglected. If β is not given, the default value in Table E-3 ($\beta = 100$) is used; "the range of β" means the range in Table E-3 (100–300 for the small-signal npn). The temperature dependence of V_{BE} is in the note to Table E-3, and the standard resistor values (E24) are in Table E-6. The circuits in this chapter contain no capacitors. Every solution starts with the active-region assumption and is checked with $V_{CE} > V_{CE(\text{sat})}$. Resistances are in kilohms, currents in milliamperes and voltages in volts.

Fixed (single base resistor) bias

6.1

★☆☆ Solution →



In the fixed-bias (single base resistor) stage shown, $V_{CC} = 15\ \text{V}$, $R_B = 1.2\ \text{M}\Omega$, $R_C = 5.1\ \text{k}\Omega$.

a. For $\beta = 160$, find I_C and V_{CE}.

b. If the transistor is replaced by another one of the same type with $\beta = 240$, what are I_C and V_{CE}?

c. At what value of β does the transistor enter saturation?

6.2 ★☆☆ Solution →

Which of the following is true for a fixed-bias (single base resistor) circuit with the emitter grounded?

A) Since $I_C \approx \beta(V_{CC} - 0.7)/R_B$, doubling β also roughly doubles I_C.

B) Increasing R_B increases I_C.

C) I_C is independent of β; the Q point shifts only because V_{BE} changes with temperature.

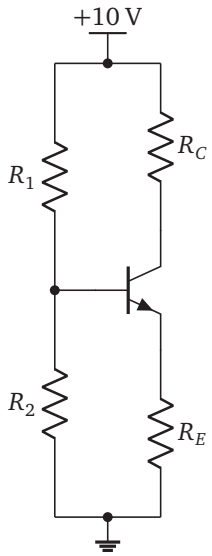
D) In this circuit the transistor cannot saturate, however large R_C is chosen.

E) Adding a resistor in the emitter increases the sensitivity of I_C to β.

pnp biasing and choice of the Q point

6.10 ★★★ Solution →

The stage shown has no capacitors; with a signal added at the base, v_{CE} moves along the dc load line. The values are $V_{CC} = 10\ \text{V}$, $R_C = 3\ \text{k}\Omega$, $R_E = 750\ \Omega$, $R_1 = 68\ \text{k}\Omega$, $R_2 = 15\ \text{k}\Omega$, $\beta = 150$. In cutoff $v_{CE} = V_{CC}$, and in saturation $v_{CE} = 0.2\ \text{V}$.



a. Find the Q point (I_C, V_{CE}) that allows the largest possible swing of v_{CE}, equal in both directions, and the peak value of this swing.

b. Find the actual Q point of the circuit and the largest symmetrical peak swing that v_{CE} can have without clipping; compare it with the ideal value in part a.

c. What is the symmetrical swing if β is at the ends of the range in Table E-3 (100 and 300)?

CHAPTER 8

MOSFETS AND JFETS: STRUCTURE, CHARACTERISTICS AND DC ANALYSIS

NMOS, saturation ($v_{DS} \geq v_{OV}$)

$$i_D = \tfrac{1}{2}k_n v_{OV}^2, \quad v_{OV} = v_{GS} - V_t, \quad k_n = k_n' \frac{W}{L}$$

NMOS, triode ($v_{DS} < v_{OV}$)

$$i_D = k_n\left(v_{OV}v_{DS} - \tfrac{1}{2}v_{DS}^2\right), \quad r_{DS} \approx \frac{1}{k_n v_{OV}}$$

channel-length modulation

$$i_D = \tfrac{1}{2}k_n v_{OV}^2(1 + \lambda v_{DS}), \quad \lambda = 1/V_A$$

body effect $\quad V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$

PMOS $\quad i_D = \tfrac{1}{2}k_p(v_{SG} - |V_t|)^2, \quad v_{SD} \geq v_{SG} - |V_t|$

JFET (n-channel), saturation

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2, \quad v_{DS} \geq v_{GS} - V_P$$

source-resistor bias

$$V_{GS} = V_G - I_D R_S \;\Rightarrow\; \text{quadratic equation}$$

CMOS inverter, switching threshold

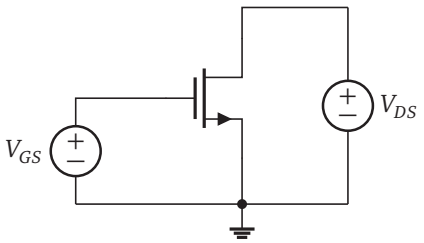
$$V_M = \frac{V_{DD} - |V_{tp}| + rV_{tn}}{1 + r}, \quad r = \sqrt{\frac{k_n}{k_p}}$$

Total instantaneous values are written with a lowercase letter and an uppercase subscript (i_D, v_{GS}), dc values with an uppercase letter and an uppercase subscript (I_D, V_{GS}). Unless stated otherwise, the discrete NMOS is the small-signal NMOS of Table E-4 ($k_n = k_n'(W/L) = 4$ mA/V^2, $V_t = 1$ V), the PMOS has $k_p = 2$ mA/V^2, $V_t = -1$ V, and the n-channel JFET has $I_{DSS} = 8$ mA, $V_P = -4$ V. Channel-length modulation (λ) and the body effect are taken into account only when the problem asks for them; the gate current is zero. Every dc solution starts with an assumed region and checks it at the end: the saturation condition is $V_{DS} \geq V_{OV}$ for the NMOS, $V_{SD} \geq V_{SG} - |V_t|$ for the PMOS and $V_{DS} \geq V_{GS} - V_P$ for the JFET. The overdrive voltage V_{OV} is written positive for the PMOS as well: $V_{OV} = V_{SG} - |V_t|$. Standard resistor values (E24) are in Table E-6. Resistances are in kilohms (gate resistors in megohms), currents in milliamperes, voltages in volts; k_n is in milliamperes per volt squared (mA/V^2).

MOSFET structure and characteristics

8.2 ★☆☆ Solution →

For the NMOS in the figure, $k_n = 6$ mA/V^2, $V_t = 1.2$ V; two dc sources set the voltages V_{GS} and V_{DS} directly.



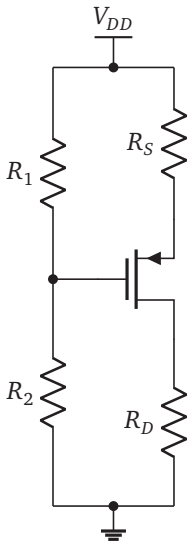
a. For (V_{GS}, V_{DS}) = (0.9 V, 5 V), (2.0 V, 3.0 V) and (2.7 V, 0.6 V), find the region of operation and I_D.

b. At $V_{GS} = 2.7$ V, what is the drain-to-source resistance (r_{DS}) for very small V_{DS} (in ohms)?

DC analysis and biasing

8.7

★★☆ Solution →



In the PMOS circuit shown, $V_{DD} = 10\,\text{V}$, $R_1 = 470\,\text{k}\Omega$, $R_2 = 680\,\text{k}\Omega$, $R_S = 1.5\,\text{k}\Omega$, $R_D = 3.9\,\text{k}\Omega$. The transistor is the small-signal PMOS of Table E-4.

a. Find I_D, V_S and V_D; check the region of operation.

b. What is the largest R_D (in kilohms) for which the transistor stays in saturation?

The MOSFET switch and the CMOS inverter

8.12

★☆☆ Solution →

Which of the following is true for a CMOS inverter?

A) With the input at 0 V, the NMOS is on and the PMOS is cut off.

B) When the output is "1", the supply delivers a continuous dc current through the PMOS even with no load connected to the output.

C) If the W/L ratio of the PMOS is reduced, the switching threshold V_M rises.

D) At $v_I = V_M$ both transistors are in the triode region.

E) With the input at 0 or at V_{DD}, the quiescent current (apart from leakage) is zero.

SOLUTIONS

3 DIODE MODELS AND DIODE CIRCUITS

3.3

← Problem

a. If both diodes are taken as short circuits, Kirchhoff's current law at node Q gives

$$\frac{9-V_Q}{1.5}+\frac{4-V_Q}{1}=\frac{V_Q}{2.2},$$

$$V_Q=\frac{9/1.5+4/1}{1/1.5+1/1+1/2.2}=\frac{10}{2.1212}=4.714\text{ V},$$

$$I_{D1}=\frac{9-4.714}{1.5}=2.857\text{ mA},$$

$$I_{D2}=\frac{4-4.714}{1}=-0.714\text{ mA}.$$

Since $I_{D2}<0$, the on assumption does not hold for D_2.

b. Assume D_2 is off and D_1 on; no current flows through R_3, and R_1 and R_2 are in series:

$$I_{D1}=\frac{9}{1.5+2.2}=2.432\approx 2.43\text{ mA},$$

$$V_Q=2.432(2.2)=5.351\approx 5.35\text{ V}.$$

Check: Here $I_{D1}>0$, and the voltage of D_2 is $V_2-V_Q=4-5.351=-1.351\text{ V}<0$: both assumptions hold.

c. With D_2 off, the value $V_Q=5.351$ V does not depend on V_2. Diode D_2 turns on when its anode (V_2) is higher than its cathode (V_Q): $V_2>5.35$ V.

Common mistake: Looking only at the positive value of I_{D1} in the solution of part a and stopping there. Each on assumption must be checked with its own current, and each off assumption with its own voltage.

ANSWER a. $V_Q=4.714$ V, $I_{D1}=2.857$ mA, $I_{D2}=-0.714$ mA; the assumption does not hold b. D_1 on, D_2 off; $V_Q=5.35$ V, $I_{D1}=2.43$ mA c. 5.35 V

3.4

← Problem

a. In the forward direction $e^{v_D/V_T}\gg 1$, so $V_D=V_T\ln(I_D/I_S)$:

$$V_D=0.025\ln\frac{0.2\times10^{-3}}{10^{-15}}=0.025\ln\left(2\times10^{11}\right),$$

$$V_D=0.025(26.02)=0.6505\approx 0.651\text{ V},$$

$$V_D=0.025\ln\left(5\times10^{12}\right)=0.025(29.24)=0.731\text{ V}.$$

b. Here $V_2-V_1=nV_T\ln(I_2/I_1)=25\ln 10=57.6$ mV.

c. Here $I_2/I_1=e^{\Delta V/V_T}=e^{30/25}=e^{1.2}=3.32$.

Check: The difference between the two voltages in part a is $0.731-0.6505=0.0805$ V; from the relation, $25\ln(5/0.2)=25\ln 25=80.5$ mV.

ANSWER a. 0.651 V and 0.731 V b. 57.6 mV c. a factor of 3.32

3.12

← Problem

a. All three diodes on: $V_X=5+0.7=5.7$ V, $V_Y=5.0$ V, $V_Z=4.3$ V. The resistor currents are

$$I_{R1}=\frac{12-5.7}{2.2}=2.864\text{ mA},$$

$$I_{R2}=\frac{5}{3.3}=1.515\text{ mA},$$

$$I_{D3}=I_{R3}=\frac{4.3+6}{4.7}=2.191\text{ mA},$$

$$I_{D1}=I_{R2}+I_{D3}=3.707\text{ mA},$$

$$I_{D2}=I_{R1}-I_{D1}=-0.843\text{ mA}.$$

Since $I_{D2}<0$, the on assumption for D_2 does not hold. (Although the currents of D_1 and D_3 are positive, this solution is invalid as a whole.)

b. Assume D_2 is off and D_1 and D_3 are on: $V_X=V_Y+0.7$, $V_Z=V_Y-0.7$. The current in R_1 passes through D_1 and divides between R_2 and the D_3–R_3

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branch:

$$\frac{12-0.7-V_Y}{2.2}=\frac{V_Y}{3.3}+\frac{V_Y-0.7+6}{4.7},$$

$$V_Y\left(\frac{1}{2.2}+\frac{1}{3.3}+\frac{1}{4.7}\right)=\frac{11.3}{2.2}-\frac{5.3}{4.7},$$

$$V_Y=\frac{4.0087}{0.9703}=4.131\text{ V},$$

$$V_X=4.831\approx 4.83\text{ V},\qquad V_Z=3.431\approx 3.43\text{ V},$$

$$I_{D1}=\frac{12-4.831}{2.2}=3.259\approx 3.26\text{ mA},$$

$$I_{D3}=\frac{3.431+6}{4.7}=2.007\approx 2.01\text{ mA}.$$

Check: Here $I_{R2}=4.131/3.3=1.252$ mA and $1.252+2.007=3.259\text{ mA}=I_{D1}$. The voltage of D_2 is $V_X-5=-0.169\text{ V}<0.7\text{ V}$: the off assumption is correct. The numerical solution with the exponential model gives $V_X=4.844$ V, $I_{D1}=3.253$ mA.

c. With D_2 off, $V_X=4.831$ V does not depend on the rail. Diode D_2 conducts when the rail voltage falls below $V_X-0.7=4.13$ V.

Common mistake: Accepting part a by looking only at the currents of D_1 and D_3. The state assumption is checked for all diodes together; if one does not hold, all values are recalculated.

ANSWER a. $I_{D1}=3.707$ mA, $I_{D2}=-0.843$ mA, $I_{D3}=2.191$ mA; does not hold b. D_2 off; $V_X=4.83$ V, $V_Y=4.13$ V, $V_Z=3.43$ V, $I_{D1}=3.26$ mA, $I_{D3}=2.01$ mA c. 4.13 V

6 BJT BIASING AND BIAS STABILITY

6.1

← Problem

Assumptions: The BJT is in the active region.

a. Base loop (1.2 MΩ = 1200 kΩ):

$$I_B=\frac{15-0.7}{1200}=11.92\ \mu\text{A},$$

$$I_C=160(11.92\ \mu\text{A})=1.907\approx 1.91\text{ mA},$$

$$V_{CE}=15-1.907(5.1)=5.28\text{ V}>0.2\text{ V}.$$

b. I_B is independent of β; I_C increases in proportion to β:

$$I_C=240(11.92\ \mu\text{A})=2.86\text{ mA},$$

$$V_{CE}=15-2.860(5.1)=0.414\text{ V}.$$

Since $V_{CE}>0.2$ V, the transistor is still active, but it is on the verge of saturation. When β increased by 50%, I_C also increased by 50%.

c. At the edge of saturation, $I_C=(15-0.2)/5.1=2.902$ mA:

$$\beta=\frac{2.902}{0.011917}=243.5.$$

Note: In Table E-3 the β range of the small-signal npn is 100–300; this circuit saturates with transistors in the upper part of the range.

ANSWER a. $I_C=1.91$ mA, $V_{CE}=5.28$ V b. 2.86 mA, 0.414 V (barely active) c. $\beta=243.5$

6.2

← Problem

The base current is set only by R_B and V_{CC}: $I_B=(V_{CC}-0.7)/R_B$. Since the collector current is βI_B, it is directly proportional to β. **A** is correct.

- (B): As R_B increases, I_B, and hence I_C, decreases.
- (C): The real problem is β; a 0.1 V change in V_{BE} is small compared with $V_{CC}-0.7$.
- (D): As R_C increases, $V_{CE}=V_{CC}-I_CR_C$ falls; the transistor saturates when $\beta I_BR_C>V_{CC}-0.2$.
- (E): It is the other way round; an emitter resistor ($I_B=(V_{CC}-0.7)/(R_B+(\beta+1)R_E)$) reduces the sensitivity by decreasing I_B when β increases.

ANSWER A

6.10

← Problem

Assumptions: The BJT is in the active region; since there are no capacitors, the signal moves the Q point along the dc load line.

a. The load line is $V_{CE}=10-I_CR_{\text{dc}}$, with $R_{\text{dc}}=R_C+R_E/\alpha=3+0.75(151/150)=3.755$ kΩ. The swing toward cutoff is $V_{CC}-V_{CE}$, the swing toward saturation is $V_{CE}-0.2$; the two must be equal:

$$V_{CE}=\frac{V_{CC}+0.2}{2}=5.10\text{ V},$$

$$I_C=\frac{10-5.1}{3.755}=1.305\text{ mA}.$$

The peak swing is $5.1-0.2=4.90$ V.

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b. Thévenin: $V_{\text{Th}} = 10(15/83) = 1.807$ V, $R_{\text{Th}} = 68 \parallel 15 = 12.29$ kΩ;

$$I_B = \frac{1.807 - 0.7}{12.29 + 151(0.75)} = \frac{1.107}{125.5} = 8.820\ \mu\text{A},$$

$$I_C = 1.323\ \text{mA}, \quad I_E = 1.332\ \text{mA},$$

$$V_{CE} = 10 - 1.323(3) - 1.332(0.75) = 5.03\ \text{V}.$$

Since $V_{CE} > 0.2$ V, the transistor is active. The swing toward cutoff is $10 - 5.032 = 4.968$ V and toward saturation $5.032 - 0.2 = 4.832$ V: the symmetrical swing is 4.83 V (saturation-limited), 1.4% below the ideal (4.90 V). The Q point is very close to the ideal point ($I_C = 1.305$ mA).

c. With the same relation:

$$\beta = 100: \quad I_C = 1.258\ \text{mA}, \quad V_{CE} = 5.27\ \text{V},$$

$$\beta = 300: \quad I_C = 1.395\ \text{mA}, \quad V_{CE} = 4.76\ \text{V}.$$

At $\beta = 100$ the swing is limited by cutoff: $10 - 5.274 = 4.73$ V. At $\beta = 300$ it is limited by saturation: $4.764 - 0.2 = 4.56$ V.

Check: Both swings are smaller than the ideal 4.90 V of part a: by 3.6% at $\beta = 100$ and by 6.9% at $\beta = 300$.

Note: The divider and R_E keep the Q point near the middle of the load line even though β changes by a factor of three.

ANSWER a. $I_C = 1.305$ mA, $V_{CE} = 5.10$ V, 4.90 V b. $I_C = 1.323$ mA, $V_{CE} = 5.03$ V, 4.83 V c. 4.73 V ($\beta = 100$), 4.56 V ($\beta = 300$)

8 MOSFETS AND JFETS: STRUCTURE, CHARACTERISTICS AND DC ANALYSIS

8.2

← Problem

a. The region is chosen with $V_{OV} = V_{GS} - V_t$ (note to Table E-4):

(0.9 V, 5 V): $V_{OV} = -0.3\ \text{V} < 0$; there is no channel, **cutoff**, $I_D = 0$.

(2.0 V, 3.0 V): $V_{OV} = 0.8$ V, $V_{DS} = 3.0\ \text{V} \geq 0.8$ V, **saturation**:

$$I_D = \tfrac{1}{2}(6)(0.8)^2 = 1.92\ \text{mA}.$$

(2.7 V, 0.6 V): $V_{OV} = 1.5$ V, $V_{DS} = 0.6\ \text{V} < 1.5$ V, **triode**:

$$I_D = 6\big(1.5(0.6) - \tfrac{1}{2}(0.6)^2\big) = 6(0.72) = 4.32\ \text{mA}.$$

b. At small v_{DS}, $i_D \approx k_n V_{OV} v_{DS}$:

$$r_{DS} = \frac{1}{k_n V_{OV}} = \frac{1}{6(1.5)} = 0.1111\ \text{k}\Omega = 111\ \Omega.$$

Check: In the second case saturation begins at $V_{DS} = V_{OV} = 0.8$ V; at this point the triode relation also gives $6(0.8 \cdot 0.8 - 0.32) = 1.92$ mA (the two relations meet at the boundary).

ANSWER a. cutoff, 0; saturation, 1.92 mA; triode, 4.32 mA b. 111 Ω

8.7

← Problem

Assumptions: The PMOS is in saturation; $\lambda = 0$.

a. Table E-4: $k_p = 2\ \text{mA/V}^2$, $|V_t| = 1$ V. Gate divider:

$$V_G = 10\,\frac{680}{1150} = 5.913\ \text{V}.$$

Source voltage and source-to-gate voltage:

$$V_S = 10 - 1.5 I_D,$$

$$V_{SG} = V_S - V_G = 4.087 - 1.5 I_D;$$

in saturation $I_D = \tfrac{1}{2}(2)V_{OV}^2 = V_{OV}^2$ and $V_{OV} = V_{SG} - 1$:

$$1.5 V_{OV}^2 + V_{OV} - 3.087 = 0,$$

$$V_{OV} = \frac{-1 + \sqrt{1 + 18.52}}{3} = 1.139\ \text{V},$$

$$I_D = (1.139)^2 = 1.298 \approx 1.30\ \text{mA}.$$

$$V_S = 10 - 1.5(1.298) = 8.05\ \text{V},$$

$$V_D = 1.298(3.9) = 5.06\ \text{V}.$$

$V_{SD} = 8.052 - 5.064 = 2.99\ \text{V} \geq V_{OV} = 1.14$ V: the saturation assumption holds.

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b. The condition $V_{SD} \geq V_{SG} - |V_t|$ means $V_D \leq V_G + |V_t| = 6.913$ V; I_D does not depend on R_D:

$$R_D \leq \frac{6.913}{1.298} = 5.32\ \text{k}\Omega.$$

Check: $V_{SG} = 8.052 - 5.913 = 2.139$ V, $V_{OV} = 1.139$ V, $\frac{1}{2}(2)(1.139)^2 = 1.298$ mA.

ANSWER a. $I_D = 1.30$ mA, $V_S = 8.05$ V, $V_D = 5.06$ V; saturation b. 5.32 kΩ

8.12

← Problem

With the input at 0, the NMOS has $v_{GS} = 0 < V_{tn}$ (cutoff); with the input at V_{DD}, the PMOS has $v_{SG} = 0 < |V_{tp}|$ (cutoff). Since there is no current path, the current of the conducting transistor is zero; $i_D = 0$ in the triode region means $v_{DS} = 0$, and the output sits at the rail itself. **E** is correct.

- (A): The reverse: with the input at 0 the PMOS is on ($v_{SG} = V_{DD}$) and the NMOS is cut off; the output is V_{DD}.
- (B): With the output at "1" the NMOS is cut off; there is no dc current (this is the origin of the low static power of CMOS).
- (C): As k_p decreases, the PMOS becomes weaker, $r = \sqrt{k_n/k_p}$ increases and V_M falls.
- (D): At V_M both transistors are in saturation; this is the steepest part of the VTC.

ANSWER E

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APPENDIX: TABLES

The tables in this appendix are used to solve the problems. The values are **typical, rounded** values chosen from physical constants, measured material data, the IEC 60063 standard values and general data-sheet ranges; they are not the data of a particular product. When a problem does not give a parameter, the **default** value of this appendix (bold in the tables) is used: room temperature 300 K, $V_T = 25$ mV, $V_{D0} = 0.7$ V for a Si diode, $V_{BE(\text{on})} = 0.7$ V, $V_{CE(\text{sat})} = 0.2$ V and $\beta = 100$ for a BJT (50 for a power BJT, Table E-3); $r_o = \infty$ unless V_A or λ is given; $k_n = 4$ mA/V^2, $V_t = 1$ V for a discrete MOSFET and $I_{DSS} = 8$ mA, $V_P = -4$ V for a JFET (Table E-4); the op amp is ideal unless stated otherwise. Values not in a table are found by **linear interpolation**: if $x_1 < x < x_2$, then $y = y_1 + (y_2 - y_1)(x - x_1)/(x_2 - x_1)$. Table numbers are shared by the two books; this book contains E-1–E-7.

This sample includes only the Appendix tables used by the selected problems (E-2, E-3, E-4). The Appendix of the full book has 7 tables on 6 pages: physical constants and semiconductor data, diode, BJT, MOSFET, and JFET parameters, a small-signal summary, standard resistor and capacitor values, and a decibel chart with Bode rules.

Table E-2 Diode model parameters

(a) Diode types

Type	I_S	n	n range	V_D (current)	Constant drop	Piecewise-linear			$V_{R,\max}$	$I_{F,\max}$
	A			V	V_{D0} (V)	V_{D0} (V)	r_D (Ω)	range	V	A
Small-signal (Si)	10^{-15}	1.00	1–2	0.691 (1 mA)	0.7	0.684	6.40	1 mA–10 mA	100	0.2
Rectifier, power (Si)	2×10^{-8}	2.00	1.5–2	0.886 (1 A)	0.8	0.758	0.128	100 mA–1 A	50–1000	1–3
Schottky	10^{-7}	1.05	1–1.1	0.302 (10 mA)	0.3	0.295	0.672	10 mA–100 mA	20–60	1

Exponential model $i_D = I_S[e^{v_D/(nV_T)} - 1]$, $V_T = 25$ mV; the V_D column is computed with this model at the current in parentheses. The piecewise-linear model ($v_D = V_{D0} + i_D r_D$) is the chord of the exponential curve over the given current range. Small-signal resistance $r_d = nV_T/I_D$. I_S roughly doubles every 5 K; at constant current $dV_D/dT \approx -2$ mV/K. Unless stated otherwise, a Si diode uses the constant-drop model with $V_{D0} = 0.7$ V.

(b) Light-emitting diode (LED), 20 mA

Color	λ	$h\nu$	V_F	V_F range	$I_{F,\max}$
	nm	eV	V	V	mA
Infrared	940	1.32	1.3	1.1–1.5	50
Red	630	1.97	2.0	1.8–2.2	30
Yellow	590	2.10	2.1	1.9–2.4	30
Green (InGaN)	525	2.36	3.1	2.8–3.5	30
Blue	470	2.64	3.2	2.9–3.6	30
White (blue + phosphor)	—	—	3.2	2.9–3.6	30

λ: peak wavelength; $h\nu = hc/\lambda$ photon energy. An LED is modeled by a constant drop (V_F); unless stated otherwise, $I_F = 20$ mA.

(c) Zener diode, 0.5 W

V_Z	I_{ZT}	r_z	V_{Z0}	$I_{Z,\max}$	TC
V	mA	Ω	V	mA	%/K
3.3	20	30	2.70	152	−0.06
4.7	20	20	4.30	106	−0.02
5.6	20	10	5.40	89	+0.02
6.2	20	7	6.06	81	+0.04
6.8	20	5	6.70	74	+0.05
8.2	20	8	8.04	61	+0.06
10	20	15	9.70	50	+0.065
12	10	25	11.75	42	+0.07
15	10	30	14.70	33	+0.075
20	5	50	19.75	25	+0.08
24	5	70	23.65	21	+0.085

V_Z: voltage at the test current I_{ZT}; model $v_Z = V_{Z0} + r_z i_Z$, $V_{Z0} = V_Z - r_z I_{ZT}$. Knee current $I_{ZK} = 0.25$ mA (all rows); $I_{Z,\max} = P_Z/V_Z$, $P_Z = 0.5$ W. TC: temperature coefficient of V_Z.

Table E-3 BJT parameters

(a) Model parameters

Type	Polarity	β range	β	$V_{BE(\text{on})}$ V	$V_{CE(\text{sat})}$ V	I_S A	V_{BE} (current) V	$\lvert V_A\rvert$ V
Small-signal	npn	100–300	**100**	0.7	0.2	10^{-15}	0.69 (1 mA)	100
Small-signal	pnp	80–250	**100**	0.7	0.2	10^{-15}	0.69 (1 mA)	50
Medium-power	npn	40–250	**100**	0.7	0.3	10^{-14}	0.72 (30 mA)	100
Power	npn	20–100	**50**	0.7	0.5	10^{-12}	0.67 (500 mA)	100
Power	pnp	20–100	**50**	0.7	0.5	10^{-12}	0.67 (500 mA)	80

Bold β: default value (when the problem does not give one). For pnp, read $V_{EB(\text{on})}$ and $V_{EC(\text{sat})}$. $\alpha = \beta/(\beta+1)$; $i_C = I_S e^{v_{BE}/V_T}$, $V_T = 25$ mV; the V_{BE} column is computed with this relation at the current in parentheses. DC solutions use $V_{BE(\text{on})} = 0.7$ V; the temperature coefficient of V_{BE} is about -2 mV/K. The Early effect ($r_o = \lvert V_A\rvert / I_C$) is included only when the problem gives V_A.

(b) Frequency, limiting and thermal values

Type	Polarity	f_T MHz	C_μ pF	$I_{C,\max}$ A	$\lvert V_{CEO}\rvert$ V	$T_{J,\max}$ °C	θ_{JC} °C/W	θ_{JA} °C/W	$P_{D,\max}$ W
Small-signal	npn	300	2	0.20	40	150	80	200	0.63 (T_A)
Small-signal	pnp	250	3	0.20	40	150	80	200	0.63 (T_A)
Medium-power	npn	100	10	1.5	60	150	10	100	1.3 (T_A)
Power	npn	3	200	10	80	150	1.5	60	83 (T_C)
Power	pnp	3	300	10	80	150	1.5	60	83 (T_C)

C_μ at $\lvert V_{CB}\rvert \approx 5$ V; $C_\pi = g_m/(2\pi f_T) - C_\mu$. $P_{D,\max} = (T_{J,\max} - 25\,^\circ\text{C})/\theta$: for small-signal and medium-power devices with ambient at 25 °C (θ_{JA}), for power devices with the case at 25 °C (θ_{JC}). With a heat sink, $T_J = T_A + P_D(\theta_{JC} + \theta_{CS} + \theta_{SA})$; with an insulating washer, $\theta_{CS} \approx 0.5$ °C/W.

Table E-4 MOSFET and JFET parameters

(a) Two example CMOS processes (integrated circuits)

Parameter	Unit	0.5 µm-like		0.18 µm-like	
		NMOS	PMOS	NMOS	PMOS
Minimum channel length $L_{\min}$	µm	0.50		0.18	
Supply V_{DD}	V	3.3		1.8	
Oxide thickness t_{ox}	nm	12		4.2	
$C_{ox} = \varepsilon_{ox}/t_{ox}$	fF/µm^2	2.88		8.22	
Effective mobility μ	cm^2/(V·s)	470	160	420	110
$k' = \mu C_{ox}$	µA/V^2	**135**	**46.0**	**345**	**90.4**
Threshold voltage V_t	V	0.65	−0.85	0.45	−0.50
$\lvert V_A' \rvert$ ($V_A = V_A' L$)	V/µm	22	15	6	8
Body-effect coefficient γ	V$^{1/2}$	0.55	0.60	0.40	0.45
$2\phi_f$	V	0.75		0.85	
Overlap capacitance C_{ov}	fF/µm	0.35		0.40	

In saturation $i_D = \frac{1}{2} k_n' (W/L)(v_{GS} - V_t)^2 (1 + \lambda v_{DS})$, $v_{DS} \geq v_{OV} = v_{GS} - V_t$; in triode $i_D = k_n' (W/L)[v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2]$. For PMOS read v_{SG}, v_{SD} and $\lvert V_t \rvert$. $\lambda = 1/\lvert V_A \rvert$; body effect $V_t = V_{t0} + \gamma[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}]$. The k' values are used directly in the problems. Channel-length modulation and the body effect are included only when the problem asks for them.

(b) Discrete MOSFET (enhancement type)

Type	k_n mA/V^2	range mA/V^2	V_t V	range V	λ V^{-1}	C_{gs} pF	C_{gd} pF	$I_{D,\max}$ A	$V_{DS,\max}$ V	$R_{DS(\text{on})}$ Ω
Small-signal NMOS	**4.0**	1–20	**1.0**	0.8–2.5	0.01	20	5	0.2	60	—
Small-signal PMOS	**2.0**	0.5–10	**−1.0**	−0.8 … −2.5	0.02	30	8	0.2	−60	—
Power NMOS (switching)	**2000**	500–5000	**3.0**	2–4	0	1500	100	20	100	0.071

$k_n = k_n' (W/L)$; bold values are the defaults. The PMOS row gives k_p; V_t and $V_{DS,\max}$ are negative. $R_{DS(\text{on})}$: drain–source resistance when fully on ($v_{GS} = 10$ V).

(c) JFET

Type	I_{DSS} mA	range mA	V_P V	range V	λ V^{-1}	g_{m0} mA/V	C_{gs} pF	C_{gd} pF
n-channel JFET	**8**	2–20	**−4.0**	−0.5 … −8	0.01	4.00	4	1.5
p-channel JFET	**6**	2–15	**3.0**	+0.5 … +6	0.01	4.00	6	2

In saturation $i_D = I_{DSS}(1 - v_{GS}/V_P)^2$, $\lvert v_{DS} \rvert \geq \lvert v_{GS} - V_P \rvert$; $g_{m0} = 2I_{DSS}/\lvert V_P \rvert$, $g_m = g_{m0}(1 - V_{GS}/V_P)$. Bold values are the defaults.

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