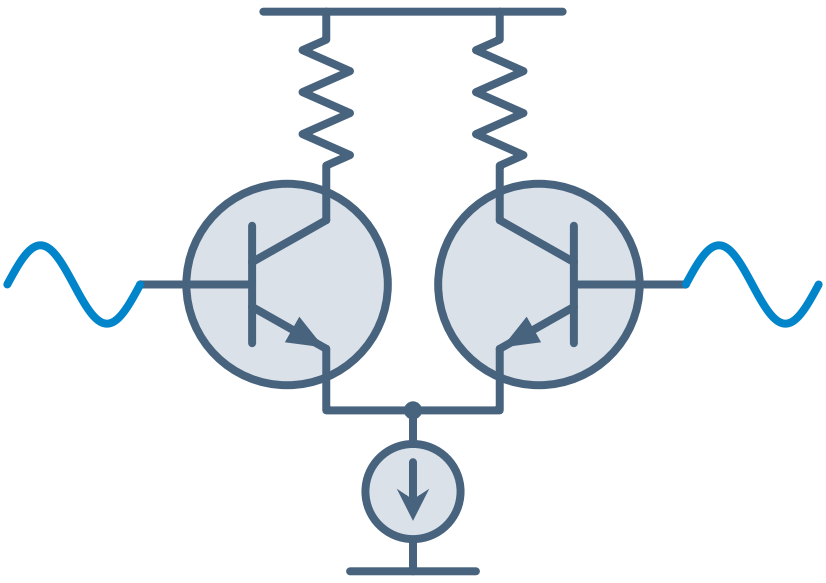
ELECTRONICS 2

PROBLEM BOOK

SAMPLE PAGES

11 chapters · 150 problems · step-by-step solutions



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How to use this book

- Each chapter opens with a reminder box summarizing the definitions and formulas the problems rely on.
- Difficulty: ★☆☆ basic ★★☆ intermediate ★★★ advanced. Each chapter has a few multiple-choice concept questions; its last problem is an exam-style mixed problem combining several topics.
- The dotted area below each problem is for your own work. Solve first; if stuck, go back to the reminder box and the lecture notes, and look at the solution last.
- All solutions are at the end of the book. The Solution → link next to a problem takes you to its solution, and ← Problem takes you back. Short answers are in the **ANSWER** box. Where needed, a solution begins with its assumptions and names the appendix tables it uses; amplifier solutions include a figure of the small-signal equivalent circuit.
- **Appendix tables:** Device parameters (BJT, MOSFET, general-purpose op amp), a small-signal summary, standard values (E12, E24), decibel and Bode rules, reference tables for feedback and output stages, and Butterworth and Chebyshev filter tables are in the appendix at the end of the book. Problems are solved with this appendix and the problem data only; a parameter not given takes its default value from the appendix.
- **Notation and defaults:** The total instantaneous value is written i_C, the dc value I_C, the small-signal value i_c and its amplitude I_c. Unless stated otherwise, $V_T = 25$ mV, $V_{BE(\text{on})} = V_{D(\text{on})} = 0.7$ V, $V_{CE(\text{sat})} = 0.2$ V, $V_A = \infty$ and $\lambda = 0$. Each dc solution starts from an assumed operating region and checks that assumption at the end.
- **Shared chapter:** Chapter 11 (frequency response) is the same as in *Electronics 1*; for schools that cover it in the first course it serves as review. Diode, BJT and MOSFET circuits and single-stage amplifiers are assumed and are summarized in the reminder boxes where needed.
- **Advanced chapter:** Chapter 21 (Active filters) is covered in only some courses and is marked ADVANCED in the contents. If your course does not cover this topic, you can skip this chapter.
- **Midterm and final:** The midterm usually covers Chapters 11–15 (frequency response, current mirrors, the differential amplifier, multistage amplifiers) and the final the whole book; topics vary from school to school, so choose the chapters according to your own syllabus. You can also verify the results with a circuit simulator.

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CHAPTER 12

CURRENT MIRRORS, CURRENT SOURCES AND ACTIVE LOADS

model (Table E-5)
$g_m = \frac{I_C}{V_T},\ g_m = \frac{2I_D}{V_{OV}},\quad r_o = \frac{V_A}{I},\ V_A = V_A' L$

BJT mirror (area ratio m)
$I_O = \frac{m\, I_{\text{REF}}}{1+(m+1)/\beta},\quad m=1:\ I_O = \frac{I_{\text{REF}}}{1+2/\beta}$

base-current-compensated mirror $I_O = \frac{I_{\text{REF}}}{1+2/[\beta(\beta+1)]}$

MOS mirror; output resistance
$I_O = I_{\text{REF}}\frac{(W/L)_2}{(W/L)_1},\quad I_O \approx I_{O0} + \frac{V_O - V_{GS}}{r_{o2}}$

Widlar source
$I_O R_E = V_T \ln\frac{I_{\text{REF}}}{I_O},\quad R_o = r_o\left[1+g_m(R_E \parallel r_\pi)\right]$

Wilson source $I_O = \frac{I_{\text{REF}}}{1+2/[\beta(\beta+2)]},\quad R_o \approx \frac{\beta r_o}{2}$

MOS cascode mirror
$R_o = 2r_o + g_m r_o^2 \approx g_m r_o^2,\quad V_{O,\min} = V_t + 2V_{OV}$

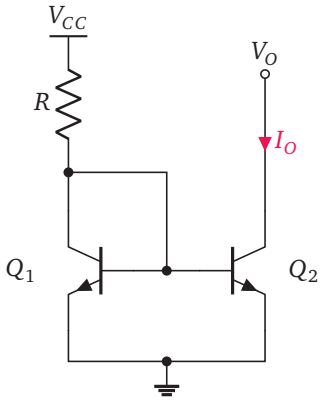
active-loaded CE and CS
$A_v = -g_{m1}(r_{o1} \parallel r_{o2}),\quad g_m r_o = \frac{V_A}{V_T}$ or $\frac{2V_A}{V_{OV}}$

In a current mirror the reference current is denoted by I_{REF}, the output current by I_O, the voltage of the output terminal by V_O and the output resistance by R_o; I_{O0} is the output current found by neglecting the Early effect. The notation is as in the previous chapters: i_C is the total instantaneous value, I_C the dc value and i_c the small-signal value. Unless stated otherwise, $V_T = 25$ mV, $V_{BE(\text{on})} = V_{EB(\text{on})} = 0.7$ V, $V_{CE(\text{sat})} = 0.2$ V; the transistors in a mirror are matched (same I_S, or same k_n' and V_t); if β is not given, the default value in Table E-3 ($\beta = 100$) is used, and if V_A or λ is not given, $r_o = \infty$. In the MOSFET saturation region $i_D = \frac{1}{2}k_n V_{OV}^2$, $k_n = k_n'(W/L)$; the body effect is neglected. Process data are in Table E-4, and the model relations and the relations with r_o in Table E-5. Resistances are in kilohms, currents in milliamperes, voltages in volts, and g_m in milliamperes per volt (mA/V).

The basic current mirror

12.2 ★☆☆ Solution →

In the current mirror shown, $V_{CC} = 9$ V, $R = 15$ kΩ; the transistors are matched, $\beta = 125$, $V_A = 75$ V.



a. What are I_{REF} and I_O (neglecting the Early effect)? By what percentage is I_O smaller than I_{REF}?

b. Find the output resistance r_{o2} and I_O when the output terminal is at $V_O = 6$ V.

Current steering

12.6 ★☆☆ Solution →

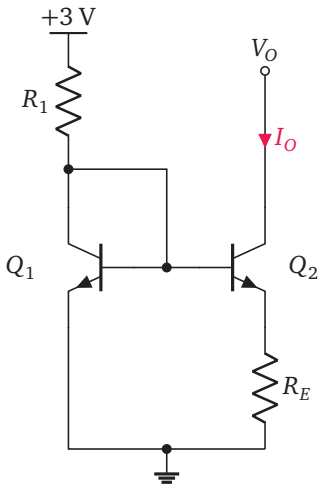
In an NMOS current-steering circuit, the reference transistor M_1 ($W/L = 4\,\mu\text{m}/0.5\,\mu\text{m}$) carries $I_{\text{REF}} = 25\,\mu\text{A}$. The drains of M_2 ($6\,\mu\text{m}/1\,\mu\text{m}$) and M_3 ($12\,\mu\text{m}/0.5\,\mu\text{m}$), which see the same gate–source voltage, are tied together and connected to a single load. What is the total current through the load? ($\lambda = 0$; all transistors in saturation.)

A) 93.8 µA **B)** 113 µA **C)** 150 µA **D)** 75.0 µA **E)** 18.8 µA

Output resistance; Widlar and Wilson sources

12.8 ★★★ Solution →

The integrated transmitter circuit of a remote control powered by a 3 V coin cell requires a bias current of 20 µA. Since a high-value resistor takes up a lot of area in an integrated circuit, the Widlar source shown will be used; $I_{\text{REF}} = 0.2$ mA is chosen. In this process resistors can be made in steps of 0.5 kΩ. Neglect the base currents.



a. Compute R_1 and R_E and round them to the nearest multiple of 0.5 kΩ.

b. What is I_O with the chosen resistors? (The equation is solved by iteration.)

c. Find the R_1 required to obtain the same current with a basic mirror; compare the total resistances of the two solutions and the currents they draw from the battery.

d. Find the output resistance with $\beta = 100$ and $V_A = 75$ V; compare it with that of a basic mirror at the same current.

CHAPTER 17

STABILITY AND FREQUENCY COMPENSATION

single pole: closed-loop pole

$$\omega_{pf} = \omega_p(1 + A_0\beta), \quad A_{f0} = \frac{A_0}{1 + A_0\beta}$$

two poles: closed-loop poles

$$s^2 + (\omega_1 + \omega_2)s + (1 + A_0\beta)\omega_1\omega_2 = 0$$

two poles: Q and ω_0

$$\omega_0 = \sqrt{(1 + A_0\beta)\omega_1\omega_2}, \quad Q = \frac{\omega_0}{\omega_1 + \omega_2}$$

peaking ($Q > 0.707$)

$$\frac{|A_f|_{\max}}{A_{f0}} = \frac{Q}{\sqrt{1 - 1/(4Q^2)}}, \quad \omega_{\text{peak}} = \omega_0\sqrt{1 - \frac{1}{2Q^2}}$$

phase margin (crossover frequency f_c: $|A\beta| = 1$)

$$\phi_M = 180^\circ + \angle A\beta(jf_c)$$

gain margin (phase-crossover frequency f_{180})

$$G_M = -20\log_{10}|A\beta(jf_{180})|$$

dominant pole and second pole ($f_c \approx \beta f_t$)

$$f_t = A_0 f_b, \quad \phi_M \approx 90^\circ - \arctan\frac{f_c}{f_{p2}}$$

Miller compensation (pole splitting)

$$f_{p1} \approx \frac{1}{2\pi g_{m2}R_2R_1C_C}, \; f_{p2} \approx \frac{g_{m2}C_C}{2\pi[C_1C_2 + C_C(C_1 + C_2)]}$$

Here β is the feedback factor and, unless stated otherwise, is independent of frequency; $A\beta$ is the loop gain. The amplifier gain is A_0 at low frequencies, its poles are given by $f_1 < f_2 < \ldots$, and the poles lie in the left half-plane; the feedback circuit is stable if all roots of $1 + A(s)\beta = 0$ lie in the left half-plane. On a Bode plot this means that the phase does not reach -180° at the frequency f_c where $|A\beta| = 1$; the phase margin ϕ_M and the gain margin G_M measure by how much this is satisfied. The unity-gain frequency of a compensated op amp is $f_t = A_0 f_b$, and in a circuit with β the loop gain falls to 1 at approximately $f_c \approx \beta f_t$. When "the op amp in Table E-8" is specified, f_t, A_0 and R_o are taken from there. The decibel chart and the Bode rules are in Table E-7, the standard values (E12, E6) in Table E-6. Here s is in rad/s and f in hertz; angles are in degrees.

Pole movement with feedback

17.2 ★☆☆ Solution →

Negative feedback with a frequency-independent β is applied to an amplifier whose gain is (s in rad/s)

$$A(s) = \frac{400}{(1 + s/2\times10^4)(1 + s/5\times10^5)}$$

Above which value of β do the closed-loop poles become complex (a conjugate pair)?

A) 0.0313

B) 0.0169

C) 0.0144

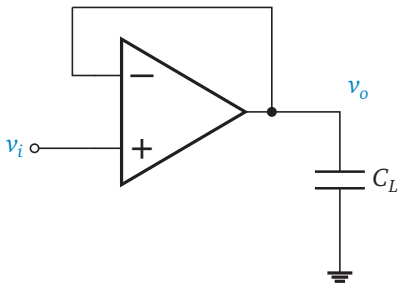
D) 0.00250

E) For no β; the closed-loop poles of a two-pole amplifier are always real.

Stability from Bode plots: gain and phase margins

17.6 ★★☆ Solution →

The output signal of an amplifier is carried to a remote display panel over a shielded cable several meters long; the cable presents a capacitive load to the voltage follower used as a buffer. The CMOS op amp in Table E-8, as a voltage follower, drives a capacitive load $C_L = 470$ pF (the cable capacitance and the panel input). The op amp is represented by a single-pole model (f_t) with an open-loop output resistance R_o.



a. Find the pole formed by R_o and C_L, and the phase margin.

b. What is the largest C_L (in pF) for a phase margin of at least 45°?

Dominant-pole compensation

17.8 ★★☆ Solution →

An amplifier has a low-frequency gain $A_0 = 1000$; its dominant pole comes from an internal node with total resistance $R = 40$ kΩ and capacitance $C = 5$ pF; the other poles are at 10 MHz and 60 MHz. The amplifier is to be used as a unity-gain follower ($\beta = 1$).

a. Where is the original dominant pole?

b. What capacitance must be added from this node to ground for $|A|$ to fall to 0 dB at 10 MHz?

c. Estimate the phase margin, taking the crossover frequency as 10 MHz.

d. If the original pole stayed in place and a new dominant pole were added, what would the open-loop bandwidth be? How many times wider is the bandwidth obtained by shifting the pole?

CHAPTER 20

OSCILLATORS, COMPARATORS AND WAVEFORM GENERATORS

Barkhausen criterion $A(j\omega_0)\beta(j\omega_0) = 1$

Wien bridge $f_0 = \dfrac{1}{2\pi RC}, \quad A \geq 3$

RC phase shift $f_0 = \dfrac{1}{2\pi\sqrt{6}RC}, \quad \dfrac{R_f}{R} \geq 29$

Colpitts $f_0 = \dfrac{1}{2\pi\sqrt{LC_1C_2/(C_1+C_2)}}, \quad g_m R \geq \dfrac{C_2}{C_1}$

Hartley $f_0 = \dfrac{1}{2\pi\sqrt{(L_1+L_2)C}}, \quad g_m R \geq \dfrac{L_1}{L_2}$

crystal $f_s = \dfrac{1}{2\pi\sqrt{L_s C_s}}, \quad f_p = f_s\sqrt{1+\dfrac{C_s}{C_p}}$

noninverting Schmitt (thresholds) $V_{TH} = -V_{TL} = L\dfrac{R_1}{R_2}$

RC charge/discharge time $t = RC\ln\dfrac{V_\infty - V_\text{i}}{V_\infty - V_\text{f}}$

square/triangle generator $\hat{V}_\text{tri} = L\dfrac{R_1}{R_2}, \quad f = \dfrac{R_2}{4R_1RC}$

555-type: thresholds $\frac{2}{3}V_{CC}$ (or V_{CV}), $\frac{1}{3}V_{CC}$ ($V_{CV}/2$)

monostable; astable

$T = RC\ln 3; \quad t_H = (R_A + R_B)C\ln 2,\ t_L = R_B C\ln 2$

Unless stated otherwise, op amps are ideal; in comparator and Schmitt circuits the output is at one of two saturation levels ($+L, -L$) and switches instantly. Typical op-amp values (output swing, slew rate) are in Table E-8, oscillator conditions in Table E-9(c), discrete MOSFET values in Table E-4, and standard values (E24) in Table E-6. Inductors L and capacitors C are lossless; in LC oscillators R is the total resistance at the output node (including the load and r_o), and the input resistance of the amplifier is infinite. In the 555-type timer the thresholds of the internal comparators are $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$; if V_{CV} is applied to the control pin, they become V_{CV} and $V_{CV}/2$. The duty cycle is the ratio of the time the output stays high to the period.

Barkhausen criterion and RC oscillators

20.2

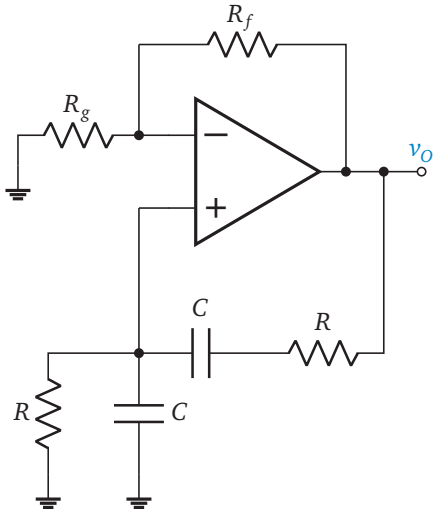
★☆☆ Solution →

In the Wien-bridge oscillator shown, $R = 12\ \text{k}\Omega$, $C = 8.2\ \text{nF}$ and $R_g = 10\ \text{k}\Omega$.

a. Find the oscillation frequency.

b. What is the minimum R_f (in kilohms) for the oscillation to be sustained?

c. If $R_f = 22\ \text{k}\Omega$ is chosen, what is the loop gain at f_0?

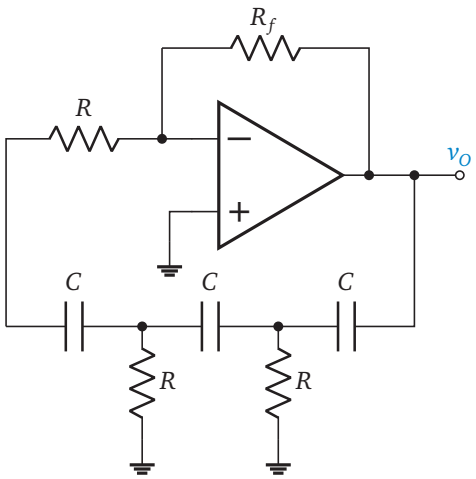


20.3 ★★☆ Solution →

In the *RC* phase-shift oscillator shown, all three capacitors are $C = 4.7$ nF; the third R is the input resistance of the inverting amplifier (it is connected to the virtual ground).

a. For an oscillation frequency of about 1.5 kHz, compute R, choose it from E24, and find f_0 with the chosen value.

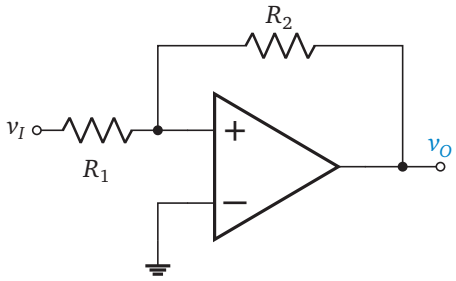
b. Find the minimum R_f; choose an E24 value so that oscillation starts, and find the loop gain at f_0.



Comparator and Schmitt trigger

20.8 ★☆☆ Solution →

In the noninverting Schmitt trigger shown, $R_1 = 10\ \text{k}\Omega$ and $R_2 = 100\ \text{k}\Omega$; the op-amp output saturates at ± 12 V. Which of the following are the input thresholds at which the output changes state?



A) ± 1.09 V **B)** ± 1.20 V **C)** ± 12.0 V **D)** 0 and $+1.20$ V **E)** ± 0.600 V

SOLUTIONS

12 CURRENT MIRRORS, CURRENT SOURCES AND ACTIVE LOADS

12.2

← Problem

Assumptions: Both transistors are in the active region; Q_1 is diode-connected ($V_{CB} = 0$).

a. The collector of Q_1 is at $V_{BE} = 0.7$ V:

$$I_{\text{REF}} = \frac{V_{CC} - V_{BE}}{R} = \frac{9 - 0.7}{15} = 0.5533 \approx 0.553 \text{ mA},$$

$$I_O = \frac{I_{\text{REF}}}{1 + 2/\beta} = \frac{0.5533}{1.016} = 0.5446 \approx 0.545 \text{ mA}.$$

The ratio is $1/1.016 = 0.9843$: I_O is 1.57% smaller than I_{REF}.

b. The relations are in Table E-5:

$$r_{o2} = \frac{V_A}{I_O} = \frac{75}{0.5446} = 137.7 \approx 138 \text{ k}\Omega,$$

$$I_O = I_{O0} + \frac{V_O - V_{BE}}{r_{o2}} = 0.5446 + \frac{6 - 0.7}{137.7}$$

$$= 0.5831 \approx 0.583 \text{ mA}.$$

Since the V_{CE} of Q_2 is 5.3 V larger than that of Q_1, the output current increases by 7.07%.

Check: The other form of the Early relation gives the same result:

$$I_{O0}\left(1 + \frac{5.3}{V_A}\right) = 0.5446(1.0707) = 0.5831 \text{ mA}.$$

Since $V_{CE2} = 6 \text{ V} > 0.2 \text{ V}$, Q_2 is in the active region.

ANSWER a. $I_{\text{REF}} = 0.553$ mA, $I_O = 0.545$ mA; 1.57% smaller b. $r_{o2} = 138$ kΩ; $I_O = 0.583$ mA

12.6

← Problem

The current scales with the W/L ratio, not with W. Here $(W/L)_1 = 8$, $(W/L)_2 = 6$, $(W/L)_3 = 24$:

$$I_2 = 25\,\tfrac{6}{8} = 18.75 \text{ μA}, \quad I_3 = 25\,\tfrac{24}{8} = 75 \text{ μA},$$

$$I_2 + I_3 = 93.75 \approx 93.8 \text{ μA}.$$

A is correct.

- (B): Only the width ratio was used ($6/4 + 12/4 = 4.5$, 112.5 μA); since the channel length of M_2 is doubled, its W/L is 0.75 times, not 1.5 times.
- (C): The transistor M_2 was also taken as $W/L = 24$ like M_3 ($2 \times 3 \times 25$); the sizes are different.
- (D) and (E): These are the current of M_3 alone (75.0 μA) or of M_2 alone (18.8 μA); when the drains are tied together, the currents add.

ANSWER A

12.8

← Problem

Assumptions: Both transistors are in the active region; the base currents are neglected; Q_1 is diode-connected ($V_{BE1} = 0.7$ V).

a. Here $R_1 = (3 - 0.7)/0.2 = 11.5$ kΩ; this is already a multiple of 0.5 kΩ. From the base–emitter loop, $V_{BE1} = V_{BE2} + I_O R_E$; with $V_{BE1} - V_{BE2} = V_T \ln(I_{\text{REF}}/I_O)$,

$$R_E = \frac{V_T}{I_O} \ln \frac{I_{\text{REF}}}{I_O} = \frac{0.025}{0.02} \ln 10 = 2.878 \approx 2.88 \text{ k}\Omega.$$

The nearest multiple of 0.5 kΩ is 3.0 kΩ (2.5 kΩ is farther away).

b. Here $I_{\text{REF}} = 2.3/11.5 = 0.200$ mA. The equation $I_O = (V_T/R_E)\ln(I_{\text{REF}}/I_O)$ is iterated (I_O in microamperes, $V_T/R_E = 8.333$ μA):
$20 \to 19.19 \to 19.53 \to 19.38 \to 19.45 \to \cdots$;

$$I_O = 8.333 \ln \frac{200}{I_O} = 19.43 \approx 19.4 \text{ μA}.$$

c. In a basic mirror $I_O \approx I_{\text{REF}}$: $R_1 = 2.3/0.02 = 115$ kΩ. The Widlar source makes do with $11.5 + 3.0 = 14.5$ kΩ; the saving is in resistor area. The battery current, however, is $0.200 + 0.019 = 0.219$ mA for the Widlar source and $0.020 + 0.020 = 0.040$ mA for the basic mirror: the Widlar source does not reduce the battery current; it saves area in the integrated circuit.

d. Here $g_{m2} = 0.01943/0.025 = 0.7772$ mA/V, $r_{\pi 2} = 100/0.7772 = 128.7$ kΩ, $r_{o2} = 75/0.01943 = 3.860$ MΩ; $R_E \parallel r_{\pi 2} = 2.932$ kΩ.

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Table E-5(c):

$$R_o = r_{o2}\left[1 + g_{m2}(R_E \parallel r_{\pi 2})\right] = 3.860(3.278),$$

$$R_o = 12.66 \approx 12.7\ \text{M}\Omega.$$

The output resistance of a basic mirror at the same current is only $r_o = 3.86$ MΩ; the emitter resistor increases R_o by a factor of 3.28.

Check: The value found satisfies the equation:

$$8.333 \ln \frac{200}{19.43} = 8.333(2.332) = 19.43\ \mu\text{A}.$$

The complete netlist solution including the Q_1 diode, R_1 and r_{o1} gives $R_o = 12.65$ MΩ; it differs from the formula by 0.04%.

ANSWER a. $R_1 = 11.5$ kΩ, $R_E = 3.0$ kΩ (computed 2.88 kΩ) b. $I_O = 19.4$ μA c. 115 kΩ; 14.5 kΩ versus 115 kΩ; battery current 0.219 mA versus 0.040 mA d. $R_o = 12.7$ MΩ (basic mirror 3.86 MΩ)

17 STABILITY AND FREQUENCY COMPENSATION

17.2

← Problem

From $1 + A\beta = 0$, the characteristic equation ($\omega_1\omega_2 = 10^{10}$):

$$s^2 + (2 \times 10^4 + 5 \times 10^5)s + (1 + 400\beta)10^{10} = 0.$$

The roots coincide when the discriminant is zero:

$$(5.2 \times 10^5)^2 = 4(1 + 400\beta)10^{10},$$

$$1 + 400\beta = 6.76 \Rightarrow \beta = \frac{5.76}{400} = 0.0144.$$

At this β the poles coincide at $s = -2.6 \times 10^5$ rad/s; for larger β they form a conjugate pair. **C** is correct.

- (A): This is the condition for $Q = 0.707$ (maximally flat response): $1 + 400\beta = (5.2 \times 10^5)^2/(2 \times 10^{10}) = 13.52$, $\beta = 0.0313$; at that point the poles are already complex.
- (B): $6.76/400 = 0.0169$; the 1 has not been subtracted.
- (D): This is $1/A_0$; it has nothing to do with the pole locations.
- (E): As β increases, the two real poles approach each other, coincide and then separate as a conjugate pair parallel to the $j\omega$ axis; but they stay in the left half-plane (a two-pole system is stable; its tendency to ring increases).

ANSWER C

17.6

← Problem

a. Table E-8: $f_t = 10$ MHz, $R_o = 200\ \Omega$. The internal source of the op amp drives C_L through R_o; a second pole is added to the loop gain ($\beta = 1$):

$$f_{CL} = \frac{1}{2\pi(200)(470 \times 10^{-12})} = 1.693\ \text{MHz}.$$

$$|A\beta| \approx \frac{f_t}{f}\frac{1}{\sqrt{1 + (f/f_{CL})^2}} = 1.$$

With $x = f^2$, $x + x^2/f_{CL}^2 = f_t^2$; in MHz, $x^2/2.867 + x - 100 = 0$:

$$x = 15.56\ \text{MHz}^2 \Rightarrow f_c = 3.944\ \text{MHz}.$$

$$\phi_M = 90^\circ - \arctan\frac{3.944}{1.693} = 90^\circ - 66.77^\circ = 23.2^\circ.$$

The phase margin is small; the output shows marked overshoot and ringing.

b. For $\phi_M = 45^\circ$, $f_c = f_{CL}$; at that frequency $|A\beta| = (f_t/f_{CL})/\sqrt{2} = 1$:

$$f_{CL} = \frac{f_t}{\sqrt{2}} = 7.071\ \text{MHz},$$

$$C_L = \frac{1}{2\pi(200)(7.071 \times 10^6)} = 112.5\ \text{pF}.$$

Since the actual load capacitance is 4.2 times this value, a series isolation resistor at the output or an op amp compensated for capacitive loads is needed.

Check: Numerical sweep with the full model, $A_0 = 10^5$ and $f_b = 100$ Hz: $f_c = 3.944$ MHz, $\phi_M = 23.2^\circ$; at $C_L = 112.5$ pF, $\phi_M = 45.0^\circ$.

ANSWER a. $f_{CL} = 1.693$ MHz, $\phi_M = 23.2^\circ$ b. $C_L \le 112.5$ pF

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17.8

← Problem

a. From the time constant of the node:

$$f_1 = \frac{1}{2\pi(40\times10^3)(5\times10^{-12})},$$

$$f_1 = 795.8\ \text{kHz}.$$

b. With the pole shifted, $|A| \approx A_0 f_1'/(10\ \text{MHz}) = 1$ at 10 MHz:

$$f_1' = \frac{10\ \text{MHz}}{1000} = 10.0\ \text{kHz},$$

$$C_{\text{tot}} = \frac{1}{2\pi(40\times10^3)(10^4)} = 397.9\ \text{pF},$$

$$C_{\text{add}} = 397.9 - 5 = 392.9\ \text{pF}.$$

c. Phase contributions at 10 MHz: $\arctan(1000) = 89.94°$, $\arctan 1 = 45.00°$, $\arctan(1/6) = 9.46°$; total $-144.40°$:

$$\phi_M \approx 180° - 144.40° = 35.6°.$$

d. The new pole f_D must bring $|A|$ down to 0 dB at the original pole (795.8 kHz):

$$f_D = \frac{795.8\ \text{kHz}}{1000} = 795.8\ \text{Hz}.$$

Shifting the pole gives a bandwidth of 10.0 kHz; this is $10\,000/795.8 = 12.57$ times (the original ratio f_2/f_1) wider than the bandwidth obtained by adding a new pole: because the shifted pole disappears, the crossover can be extended up to the next pole (10 MHz).

Check: Exact calculation: $|A| = 1$ is reached at 7.814 MHz ($|A| = 0.697$ at 10 MHz); there $\phi_M = 44.7°$. The added capacitance is also confirmed from the node impedance: the pole of 40 kΩ ‖ 397.9 pF is at 10.0 kHz.

ANSWER a. 795.8 kHz b. $C_{\text{add}} = 392.9$ pF c. $\phi_M \approx 35.6°$ (exact 44.7°) d. 795.8 Hz; shifting the pole gives a 12.57 times wider bandwidth

20 OSCILLATORS, COMPARATORS AND WAVEFORM GENERATORS

20.2

← Problem

a. Table E-9(c), Wien bridge:

$$f_0 = \frac{1}{2\pi RC} = \frac{1}{2\pi(12\times10^3)(8.2\times10^{-9})},$$

$$f_0 = 1617\ \text{Hz} \approx 1.62\ \text{kHz}.$$

b. At f_0, $\beta = 1/3$; the gain of the noninverting amplifier must be $A = 1 + R_f/R_g \geq 3$:

$$R_f \geq 2R_g = 20.0\ \text{k}\Omega.$$

c. Gain and loop gain:

$$A = 1 + \frac{22}{10} = 3.20, \qquad A\beta = \frac{3.20}{3} = 1.067 \approx 1.07.$$

The loop gain is 6.7% greater than 1: oscillation starts reliably, and its amplitude is limited by the saturation of the op amp.

Check: Setting up $\beta(j\omega)$ of the feedback network by nodal analysis and searching for the zero-phase frequency gives 1617 Hz and $\beta = 0.3333$.

ANSWER a. $f_0 = 1.62$ kHz b. 20.0 kΩ c. 1.07

20.3

← Problem

a. Table E-9(c): $f_0 = 1/(2\pi\sqrt{6}RC)$.

$$R = \frac{1}{2\pi\sqrt{6}f_0 C} = \frac{1}{2\pi\sqrt{6}(1500)(4.7\times10^{-9})},$$

$$R = 9.216 \approx 9.22\ \text{k}\Omega.$$

The nearest E24 value is 9.1 kΩ:

$$f_0 = \frac{1}{2\pi\sqrt{6}(9.1\times10^3)(4.7\times10^{-9})} = 1519\ \text{Hz}.$$

b. At f_0 the gain of the network is $-1/29$; the gain of the inverting amplifier is $-R_f/R$:

$$R_f \geq 29R = 29(9.1) = 263.9 \approx 264\ \text{k}\Omega.$$

For startup, the first E24 value above this limit, 270 kΩ, is chosen:

$$A\beta = \frac{R_f}{29R} = \frac{270}{263.9} = 1.023 \approx 1.02.$$

Check: Setting up the three-section network and the virtual ground by nodal analysis and finding the

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frequency at which the imaginary part of the loop gain is zero gives 1519 Hz and $A\beta = 1.023$.

Common mistake: Assuming that each section shifts the phase by 60°. The sections load one another; at f_0 the shifts are 55.8°, 56.4° and 67.8° (total 180°). The result $f_0 = 1/(2\pi\sqrt{6}RC)$ is obtained with this loading; the tan 60° condition computed with unloaded sections gives the wrong frequency.

ANSWER a. $R = 9.22\ \text{k}\Omega \rightarrow 9.1\ \text{k}\Omega$, $f_0 = 1519\ \text{Hz}$
b. $R_f \geq 264\ \text{k}\Omega$, $270\ \text{k}\Omega$; $A\beta = 1.02$

20.8

← Problem

The inverting input is grounded; the output changes with the sign of the noninverting input. While $v_O = +12\ \text{V}$, the noninverting input is the tap of the divider between v_I and v_O:

$$v_+ = \frac{v_I R_2 + v_O R_1}{R_1 + R_2} = 0 \implies v_I = -v_O \frac{R_1}{R_2}.$$

With the output at +12 V, it changes at $v_I = -12(10/100) = -1.20\ \text{V}$; with the output at −12 V, at +1.20 V. The thresholds are ±1.20 V and the hysteresis width is 2.40 V. **B** is correct.

- (A): $12(10/110) = 1.09\ \text{V}$ is the divider relation of the inverting Schmitt; here the input is applied at the end of the divider.
- (C): This is the saturation level itself.
- (D): The thresholds are symmetric about zero; no reference voltage is connected to the inverting input.
- (E): This is one quarter of the hysteresis width; the threshold is LR_1/R_2, not $LR_1/(2R_2)$.

ANSWER B

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APPENDIX: TABLES

The tables in this appendix are used to solve the problems. The values are **typical, rounded** values chosen from physical constants, measured material data, the IEC 60063 standard values and general data-sheet ranges; they are not the data of a particular product. When a problem does not give a parameter, the **default** value of this appendix (bold in the tables) is used: room temperature 300 K, $V_T = 25$ mV, $V_{D0} = 0.7$ V for a Si diode, $V_{BE(\text{on})} = 0.7$ V, $V_{CE(\text{sat})} = 0.2$ V and $\beta = 100$ for a BJT (50 for a power BJT, Table E-3); $r_o = \infty$ unless V_A or λ is given; $k_n = 4$ mA/V^2, $V_t = 1$ V for a discrete MOSFET and $I_{DSS} = 8$ mA, $V_P = -4$ V for a JFET (Table E-4); the op amp is ideal unless stated otherwise. Values not in a table are found by **linear interpolation**: if $x_1 < x < x_2$, then $y = y_1 + (y_2 - y_1)(x - x_1)/(x_2 - x_1)$. Table numbers are shared by the two books; this book contains E-3–E-10.

This sample includes only the Appendix tables used by the selected problems (E-5, E-8, E-9). The Appendix of the full book has 8 tables (E-3 to E-10) on 7 pages: BJT, MOSFET, and JFET parameters, a small-signal summary, standard values, decibel and Bode rules, op-amp parameters, criteria tables for feedback, output stages, and oscillators, and Butterworth and Chebyshev filter tables.

Table E-5 Small-signal summary

(a) Model parameters

Device	Quantity	Relation
BJT	g_m	I_C/V_T
	r_π	$\beta/g_m = V_T/I_B$
	r_e	$\alpha/g_m = V_T/I_E$
	r_o	V_A/I_C
	$C_\pi + C_\mu$	$g_m/(2\pi f_T)$
MOSFET	g_m	$k_n V_{OV} = \sqrt{2k_n I_D} = 2I_D/V_{OV}$
	r_o	$V_A/I_D = 1/(\lambda I_D)$, $V_A = V'_A L$
	g_{mb}	χg_m, $\chi = \gamma/(2\sqrt{2\phi_f + V_{SB}})$
	C_{gs}, C_{gd}	$\frac{2}{3}WLC_{ox} + WC_{ov}$, WC_{ov}
	f_T	$g_m/[2\pi(C_{gs} + C_{gd})]$
JFET	g_m	$(2I_{DSS}/\lvert V_P\rvert)(1 - V_{GS}/V_P) = 2\sqrt{I_{DSS} I_D}/\lvert V_P\rvert$

(b) The six basic stages (r_o neglected)

Stage	Input	Into input terminal	R_{out}	$A_v = v_o/v_i$
Common-emitter (CE)	base	$R_{\text{base}} = (\beta + 1)(r_e + R_E)$	R_C	$-\dfrac{\alpha(R_C \parallel R_L)}{r_e + R_E}$
Common-base (CB)	emitter	$R_{\text{emitter}} = r_e$	R_C	$\dfrac{\alpha(R_C \parallel R_L)}{r_e} = g_m(R_C \parallel R_L)$
Common-collector (CC, emitter follower)	base	$R_{\text{base}} = (\beta + 1)(r_e + R_E \parallel R_L)$	$R_E \parallel \left(r_e + \dfrac{R'_s}{\beta + 1}\right)$	$\dfrac{R_E \parallel R_L}{R_E \parallel R_L + r_e}$
Common-source (CS)	gate	$R_{\text{gate}} = \infty$	R_D	$-\dfrac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$
Common-gate (CG)	source	$R_{\text{source}} = 1/g_m$	R_D	$g_m(R_D \parallel R_L)$
Common-drain (CD, source follower)	gate	$R_{\text{gate}} = \infty$	$R_S \parallel (1/g_m)$	$\dfrac{R_S \parallel R_L}{R_S \parallel R_L + 1/g_m}$

v_i: voltage at the input terminal (base, emitter, gate or source). The resistance into the input terminal is that of the transistor terminal alone (R_{base}, R_{emitter}, …). The total input resistance of the stage includes the bias resistor: $R_{\text{in}} = R_B \parallel R_{\text{base}}$ (CE, CC; $R_B = R_1 \parallel R_2$), $R_{\text{in}} = R_E \parallel R_{\text{emitter}}$ (CB), $R_{\text{in}} = R_S \parallel R_{\text{source}}$ (CG), $R_{\text{in}} = R_G$ (CS, CD). R_{out} is the output resistance of the stage (excluding R_L). R_E, R_S: unbypassed (degeneration) resistor; set to zero when bypassed (CE: $R_{\text{base}} = r_\pi$, $A_v = -g_m(R_C \parallel R_L)$). In the CC and CD rows, R_E and R_S connect the output terminal to ground; $R'_s = R_s \parallel R_B$. R_s: internal resistance of the signal source. Overall gain from source to load $G_v = A_v R_{\text{in}}/(R_{\text{in}} + R_s)$. Body effect neglected.

(c) Relations including r_o

Case	Relation
Intrinsic gain	$A_0 = g_m r_o$ (BJT: V_A/V_T; MOS: $2V_A/V_{OV}$)
CE and CS with r_o	$A_v = -g_m(R_C \parallel R_L \parallel r_o)$, $R_{\text{out}} = R_C \parallel r_o$
Degenerated BJT, looking into collector	$R_o = r_o + (R_E \parallel r_\pi)(1 + g_m r_o) \approx r_o[1 + g_m(R_E \parallel r_\pi)]$
Degenerated MOSFET, looking into drain	$R_o = r_o + R_S + g_m r_o R_S \approx r_o(1 + g_m R_S)$
Cascode (MOS; BJT)	$R_o \approx g_{m2} r_{o2} r_{o1}$; $R_o \approx g_{m2} r_{o2}(r_{o1} \parallel r_{\pi 2}) \lesssim \beta r_o$

Cascode: the lower transistor (1) is common-emitter/source, the upper one (2) common-base/gate. The output resistance of a BJT cascode is at most about βr_o.

Table E-8 Typical op-amp parameters (25 °C)

Parameter	Symbol	Unit	BJT input, general purpose	CMOS input, rail-to-rail	Ideal
Open-loop dc gain	A_0	V/V (dB)	2×10^5 (106)	10^5 (100)	∞
Unity-gain frequency	f_t	MHz	1.0	10	∞
Open-loop 3-dB frequency	$f_b = f_t/A_0$	Hz	5.0	100	∞
Slew rate	SR	V/µs	0.5	10	∞
Input offset voltage (max)	V_{OS}	mV	1 (≤ 5)	0.5 (≤ 2)	0
Drift of V_{OS}	$\Delta V_{OS}/\Delta T$	µV/K	5	2	0
Input bias current	I_B		100 nA	1 pA	0
Input offset current	I_{OS}		10 nA	0.5 pA	0
Differential input resistance	R_{id}		2 MΩ	10^{12} Ω	∞
Open-loop output resistance	R_o	Ω	75	200	0
Common-mode rejection ratio	CMRR	dB	90	80	∞
Power-supply rejection ratio	PSRR	dB	90	85	∞
Output swing	$V_{o,\max}$		$\pm(V_S - 1.5)$ V	0.05 V from the rails	rails
Output short-circuit current	I_{sc}	mA	25	40	—
Supply voltage	V_S		±5 … ± 18 V	2.7 … 5.5 V	—

Single-pole model $A(s) = A_0/(1 + s/\omega_b)$, $f_t = A_0 f_b$; closed-loop bandwidth $f_{3\text{dB}} = f_t/(1 + R_2/R_1)$ (noninverting and inverting). Full-power bandwidth $f_M = \text{SR}/(2\pi V_{o,\max})$: e.g. for the BJT-input type with $V_{o,\max} = 13.5$ V (±15 V supplies), 5.89 kHz; for the CMOS type with 2.45 V (single 5 V supply, centered at 2.5 V), 650 kHz. The swing of the BJT-input type is for $R_L \geq 2$ kΩ, that of the CMOS type for $R_L \geq 10$ kΩ. Unless stated otherwise the op amp is ideal; when a problem says “typical”, this table is used.

Table E-9 Criteria tables

(a) Feedback topologies

Amplifier	Topology	Sensing	Mixing (at input)	A	β	R_{if}	R_{of}
Voltage	series–shunt	output voltage (shunt)	voltage (series)	V/V	V/V	$R_i(1+A\beta)$	$R_o/(1+A\beta)$
Current	shunt–series	output current (series)	current (shunt)	A/A	A/A	$R_i/(1+A\beta)$	$R_o(1+A\beta)$
Transconductance	series–series	output current (series)	voltage (series)	A/V	V/A	$R_i(1+A\beta)$	$R_o(1+A\beta)$
Transresistance	shunt–shunt	output voltage (shunt)	current (shunt)	V/A	A/V	$R_i/(1+A\beta)$	$R_o/(1+A\beta)$

$A_f = A/(1+A\beta)$; loop gain $T = A\beta$; bandwidth and distortion change by the factor $(1+A\beta)$; $dA_f/A_f = (dA/A)/(1+A\beta)$. A series connection raises the resistance by $(1+A\beta)$, a shunt connection lowers it. R_i, R_o: input and output resistances of the A circuit including the loading of the feedback network.

(b) Output stage classes

Class	Conduction angle	Max. efficiency (%)	Transistor dissipation	Distortion
A (resistive or current-source load)	360°	25	largest at zero signal: $P_D = V_{CC}I_Q$	low
A (transformer or inductor coupled)	360°	50	largest at zero signal	low
B	180°	78.5	$P_{D,\max}/P_{L,\max} = 0.405$	crossover distortion
AB	180–360°	≈ 78.5	close to B, plus $V_{CC}I_Q$	small
C	$< 180°$	$\to 100$	small (tuned load)	high; filtered by the tuned circuit
D	switching	$\to 100$ (in practice > 90)	switching loss	small after filtering

Class B push–pull, $\pm V_{CC}$ supplies, load R_L, peak output $\hat{V}_o$: $P_L = \hat{V}_o^2/(2R_L)$, $P_S = 2V_{CC}\hat{V}_o/(\pi R_L)$, $\eta = (\pi/4)(\hat{V}_o/V_{CC})$. The total transistor dissipation is largest at $\hat{V}_o = 0.637V_{CC}$ $(2V_{CC}/\pi)$: $P_{D,\max} = 2V_{CC}^2/(\pi^2 R_L)$, with $\eta = 50\%$ there. The efficiencies are theoretical limits (saturation voltages neglected).

(c) Oscillator conditions

Oscillator	Frequency	Condition	Configuration
Barkhausen criterion	$A(j\omega_0)\beta(j\omega_0) = 1$	$\lvert A\beta\rvert = 1,\ \angle A\beta = 0°$	$\lvert A\beta\rvert$ slightly above 1 for startup
Wien bridge	$f_0 = \dfrac{1}{2\pi RC}$	$\beta(j\omega_0) = 1/3,\ A \geq 3$	series RC + parallel RC, equal R and C; noninverting amplifier
RC phase shift	$f_0 = \dfrac{1}{2\pi\sqrt{6}RC}$	$\beta(j\omega_0) = -1/29,\ A \leq -29$	three equal sections (series C, shunt R), unloaded; inverting
Colpitts	$f_0 = \dfrac{1}{2\pi\sqrt{LC_1C_2/(C_1+C_2)}}$	$g_mR \geq C_2/C_1$	C_1 at the output (collector/drain), C_2 at the input (base/gate)
Hartley	$f_0 = \dfrac{1}{2\pi\sqrt{(L_1+L_2)C}}$	$g_mR \geq L_1/L_2$	L_1 at the output, L_2 at the input; no mutual inductance
Crystal	$f_s = \dfrac{1}{2\pi\sqrt{L_sC_s}},\ f_p = f_s\sqrt{1+C_s/C_p}$	$f_s < f < f_p$	L_s, C_s: series branch; C_p: shunt capacitance; crystal inductive

Colpitts and Hartley conditions: amplifier transconductance g_m and total resistance R at the output node (load and r_o included), infinite input resistance. The f_0 relations assume a lossless, unloaded feedback network.

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